SPECIFICATION

Please revise the paragraphs beginning at page 5, line 22 to read as follows:

--Figure 6 illustrates a phase controlled read circuit 54 that may be used to accomplish this functionality. In Figure 6, q_1 through q_8 are outputs from the register bank 52, ~~while $\ddot{y}_1$ through $\ddot{y}_8$ are~~ while ϕ_1 through ϕ_8 are the outputs of the delay locked loop 56.

The operation of the ~~controller~~ read circuit 54 is appreciated with reference to a single column of transistors. For example, consider the first column of transistors on the left side of the circuit 54. Initially, ~~the $\ddot{y}_1$ signal is high and the $\ddot{y}_2$ signal~~ the ϕ_1 signal is high and the ϕ_2 signal is low. The digital ~~high $\ddot{y}_1$ signal~~ high ϕ_1 signal is inverted and therefore turns-on PMOS transistor 74, the digital ~~low $\ddot{y}_2$ signal~~ low ϕ_2 signal turns-on PMOS transistor 76, the digital ~~high $\ddot{y}_1$ signal~~ high ϕ_1 signal causes the NMOS transistor 78 to turn-on, while the ~~inverted $\ddot{y}_2$ signal~~ inverted ϕ_2 signal has a digital high value and thereby causes the NMOS transistor 80 to turn-on.

In sum, transistors 74, 76, 78, and 80 are turned-on. The output of node 90 will now be determined by the states of transistors 82 and 84, which receive the input signal q_1. If q_1 is a digital low value, then transistor 82 turns-on and transistor 84 remains off. Transistors 74, 76, and [[78]] 82 drive a digital high signal onto the output node 90. Thus, transistors 74, 76, and [[78]] 82 operate as a set of pull-up transistors.--

Please revise the paragraph beginning at page 6, line 4 to read as follows:

--Observe that this operation occurs in the 1/8 of a cycle while ~~the $\ddot{y}_1$ signal is high and the $\ddot{y}_2$ signal~~ the ϕ_1 signal is high and the ϕ_2 signal is low. [When $\ddot{y}_1$ and $\ddot{y}_2$ are] When ϕ_1 and ϕ_2 are both high, transistors 76 and 80 will be turned-off, thereby preventing the column of transistors from driving a signal on the output node 90. However, at this point, the next column of transistors is operative. This cascaded operation is repeated for each signal phase. The output node 90, which is connected to each column of transistors, operates as a hardwired logical OR circuit.--

Please revise the paragraph beginning at page 6, line 17 to read as follows:

--A multiplexer or de-multiplexer configuration is established by selecting the size of the register bank 52 and the corresponding delay locked loop 56 ~~to drive the register bank 52~~. This flexible scheme is highly extendible to conform to the number of LVDS channels.--